CLAIMS

[0078]   *What is claimed is:*

1.   A method of receiving data comprising the acts of:

generating a data sampling clock signal

comparing a received clock signal to the data sampling clock signal

using the data sampling clock signal to sample a data signal into sampled data representing a first zone, a second zone, and a third zone of the data signal;

determining which zone of the sampled data has a transition of the data signal

indicating a direction of change for the data sampling clock signal if the first zone or the third zone has the transition.

2.   The method of claim 1 wherein using the data sampling clock signal further comprises sampling the data signal at three times the frequency of the data signal.

3.   The method of claim 1 wherein the first zone, the second zone, and the third zone of the sampled data comprise a period of the data signal.

4.   The method of claim 1 wherein generating further comprises changing the direction of the data sampling clock signal in response to the indication.

5.   The method of claim 1 wherein indicating includes indicating an up direction when the transition occurs in the first zone.

6.   The method of claim 1 wherein indicating includes means for indicating a down direction when the transition occurs in the third zone.

7.   The method of claim 1 further comprising recovering a transmitter clock signal, wherein generating the data sampling clock signal includes using the recovered transmitter clock signal.

5   8.   The method of claim 1 wherein the comparing is performed by a frequency comparator.

9.   The method of claim 8 wherein the frequency comparator acts as a frequency acquisition aid.

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10.   A receiver apparatus comprising

a phase locked loop circuit including a voltage controlled oscillator used to generate a data sampling clock signal;

a data sampler to receive the data sampling clock signal, to sample a data signal using

15   the data sampling clock signal, wherein the frequency of the data sampling clock signal is three times greater than the data signal frequency, and to output sampled data representing a first zone, a second zone, and a third zone of the data signal;

a phase detector to examine the sampled data, to determine which zone of the sampled data has a transition of the data signal, and to output a phase detector signal

20   indicating a direction of change for the data sampling clock signal if the first zone or the third zone has the transition; and

a frequency comparator that compares the frequencies of the data sampling clock produced by the voltage controlled oscillator and a reference clock signal.

25   11.   The receiver of claim 10, wherein the frequency comparator drives the data sampling clock frequency toward the reference clock signal frequency.

12.   The receiver of claim 10, wherein the frequency comparator acts as a frequency acquisition aid.

13.   The receiver of claim 10, wherein the frequency comparator is designed to have a

5   hysteresis that closely matches the capture and lock range of the phase locked loop circuit.

14.   The receiver of claim 10, wherein the frequency comparator contains a reference loop circuit; wherein the reference loop circuit is activated when the frequency difference between the reference clock and the data sampling clock signal is greater than 1000 parts per million.

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15   The receiver of claim 10, wherein the frequency comparator contains a data loop circuit; wherein the data loop circuit is activated when the frequency difference between the reference clock and the data sampling clock signal is less than 200 parts per million.

15   16.   A method of controlling a receiver to receive data comprising the steps of:
             generating a data sampling clock signal;
             sampling a data signal using the data sampling clock signal, wherein the frequency of the data sampling clock signal is three times greater than the data signal frequency, and outputting sampled data representing a first zone, a second zone, and a third zone of the data

20   signal;
             detecting the sampled data, to determine which zone of the sampled data has a transition of the data signal, and to output a phase detector signal indicating a direction of change for the data sampling clock signal if the first zone or the third zone has the transition; and

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comparing the frequencies of the data sampling clock and a reference clock signal.

17. The method of claim 16, wherein the step of comparing drives the data sampling clock frequency toward the reference clock signal frequency.

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18. The method of claim 16, wherein the step of comparing acts as a frequency acquisition aid.

19. The method of claim 16, wherein the step of comparing is designed to have a

10 hysteresis that closely matches range of the data sampling clock signal.

20. The method of claim 16, wherein the step of comparing contains a reference loop step; wherein the reference loop step is performed when the frequency difference between the reference clock and the data sampling clock signal is greater than 1000 parts per million.

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21 The method of claim 16, wherein the step of comparing contains a data loop step; wherein the data loop step is performed when the frequency difference between the reference clock and the data sampling clock signal is less than 200 parts per million.

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